Low Power System Design

Module 7 (3 hours):
Circuit-level low power techniques and power estimation basics

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Course Goals

- Understand the Circuit-level low power design techniques
  - Trend of power consumption
  - Circuit design style
  - Transistor and gate sizing
- Understand the cell characterization step for higher-level analysis
  - Cell characterization flow
- Understand the power estimation basics
  - Signal probability
Contents

- Basics of circuit-level techniques
  - Trend of power consumption
  - Types of power dissipation
  - Power and the circuit design styles
  - Transistor and gate sizing for low power
- Cell characterization for gate-level analysis
  - SPICE power analysis
  - Power characterization for digital cell library
- Power estimation basics
  - Signal probability calculation
Trend of power consumption

- Power values of processors [ISSCC]
Trend of power consumption

- Problems found on first spin of silicon in 180/130 nm

<table>
<thead>
<tr>
<th>Issue</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Functional Logic Error</td>
<td>43%</td>
</tr>
<tr>
<td>Analog Turing Issue</td>
<td>20%</td>
</tr>
<tr>
<td>Signal Integrity</td>
<td>17%</td>
</tr>
<tr>
<td>Clock Scheme Error</td>
<td>14%</td>
</tr>
<tr>
<td>Reliability Problem</td>
<td>12%</td>
</tr>
<tr>
<td>Mixed-Signal Problem</td>
<td>11%</td>
</tr>
<tr>
<td>Power Problem</td>
<td>11%</td>
</tr>
<tr>
<td>Long Path Error</td>
<td>10%</td>
</tr>
<tr>
<td>Short Path Error</td>
<td>10%</td>
</tr>
<tr>
<td>IR Drop</td>
<td>7%</td>
</tr>
<tr>
<td>Firmware</td>
<td>4%</td>
</tr>
<tr>
<td>Other</td>
<td>3%</td>
</tr>
</tbody>
</table>
Trend of power consumption

Table 9 System Functional Requirements for the PDA SOC-LP Driver

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Technology (nm)</td>
<td>101</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
<td>1</td>
<td>0.8</td>
<td>0.6</td>
<td>0.5</td>
<td>0.4</td>
</tr>
<tr>
<td>Clock Frequency (MHz)</td>
<td>300</td>
<td>450</td>
<td>600</td>
<td>900</td>
<td>1200</td>
<td>1500</td>
</tr>
<tr>
<td>Application (maximum required performance)</td>
<td>Still Image Processing</td>
<td>Real Time Video Codec (MPEG4/CIF)</td>
<td>Real Time Interpretation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Web Browser</td>
<td>TV Telephone (1:1)</td>
<td>TV Telephone (&gt;3:1)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Electric Mailing</td>
<td>Voice Recognition (Input)</td>
<td>Voice Recognition (Operation)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Scheduler</td>
<td>Authentication (Crypto Engine)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processing Performance (COPS)</td>
<td>0.3</td>
<td>2</td>
<td>14</td>
<td>77</td>
<td>461</td>
<td>2458</td>
</tr>
<tr>
<td>Required Average Power (W)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>Required Standby Power (mW)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Battery Capacity (Wh/Kg)</td>
<td>120</td>
<td>200</td>
<td>200</td>
<td>400</td>
<td>400</td>
<td>400</td>
</tr>
</tbody>
</table>

No increase in power consumption required!
Trend of power consumption

- Dynamic vs. Static

![Graph showing the trend of power consumption over years with voltage and technology node on the left and power on the right.](image-url)
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Types of power dissipation

- Dynamic power
  - By charging and discharging capacitances
- Short-circuit power
  - Due to the short duration in which both NMOS and PMOS are turned on
- Static power
  - Can be ideally ignored in CMOS, but in pseudo NMOS
- Leakage power
  - Reverse biased PN-junction current
  - Subthreshold channel conduction current
Dynamic power

\[ i_c(t) = C_L \frac{dv_c(t)}{dt} \]

\[ E_s = \int_{t_0}^{t_1} V_i(t)dt \]

\[ E_s = C_L V \int_{t_0}^{t_1} \frac{dv_c(t)}{dt} dt = C_L V \int_{t_0}^{t_1} dv_c = C_L V^2 \]

\[ E_{cap} = \int_{t_0}^{t_1} v_c(t)i_c(t)dt = C_L \int_{t_0}^{t_1} v_c(t) \frac{dv_c(t)}{dt} dt = C_L V \int_{t_0}^{t_1} v_c dv_c = \frac{1}{2} C_L V^2 \]

\[ E_c = E_s - E_{cap} = \frac{1}{2} C_L V^2 \quad (E_d \text{ is same to } E_s) \]

\[ P = E_s f = C_L V^2 f \]
Short-circuit power

- Both transistors are turned on between $v_{tn}$ and $v_{tp}$
- Factors on short-circuit current
  - The duration and slope of input signal
  - I-V curves of PMOS / NMOS
  - Output loading
- Energy dissipation
  - $E_{\text{short}} = \frac{\beta}{12} \tau (V_{tp} - V_{tn})^3$
  - $\beta$: transistor size
  - $\tau$: the duration of input signal
Impact of load capacitance

As output loading increases:

<table>
<thead>
<tr>
<th>Current envelope</th>
<th>width</th>
<th>peak</th>
<th>integration</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{\text{short}}$</td>
<td>no change</td>
<td>decrease</td>
<td>decrease</td>
</tr>
<tr>
<td>$i_{c}$</td>
<td>increase</td>
<td>increase</td>
<td>increase</td>
</tr>
<tr>
<td>$i_{\text{short}} + i_{c}$</td>
<td>increase</td>
<td>increase</td>
<td>increase</td>
</tr>
</tbody>
</table>
Impact of input slope

As input signal slope deteriorates:

<table>
<thead>
<tr>
<th>Current envelope</th>
<th>width</th>
<th>peak</th>
<th>integration</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{\text{short}}$</td>
<td>increase</td>
<td>increase</td>
<td>increase</td>
</tr>
<tr>
<td>$i_c$</td>
<td>increase</td>
<td>decrease</td>
<td>no change</td>
</tr>
<tr>
<td>$i_{\text{short}} + i_c$</td>
<td>increase</td>
<td>decrease</td>
<td>increase</td>
</tr>
</tbody>
</table>
Leakage power

- Leakage mechanisms

![Diagram showing leakage current paths in a MOSFET](image-url)
Leakage mechanisms

- $I_1$: pn reverse-bias current
- $I_2$: weak inversion (subthreshold channel leakage)
- $I_3$: Drain-Induced Barrier-Lowering (DIBL) effect
- $I_4$: Gate-Induced Drain Leakage (GIDL)
- $I_5$: punchthrough
- $I_6$: narrow-width effect
- $I_7$: gate-oxide tunneling
- $I_8$: hot-carrier injection
Two major leakage components (I)

- $I_1$ and $I_2$ are commonly known
- The others are especially important as process technology advances
- $I_1$: pn reverse-bias current
  - Minority carrier drift near the edge of the depletion region
  - Electron-hole pair generation (depl. region of the junction)
  - $I_{\text{reverse}} = I_s \left( e^{V_{th}/T} - 1 \right)$  
    \[ V_{th} = kT / q \]
- Largely depends on
  - Fabrication process
  - Junction area
  - Temperature
Two major leakage components (II)

- $I_2$: weak inversion (subthreshold channel leakage)
  - Only occurs when the gate voltage is below $V_t$
  - No horizontal electric field in this case
  - Carriers move by diffusion
    - $I_{sub} = I_0 e^{(V_{gs} - V_i)/(\alpha V_{th})}$
    - $I_0$ is the current when $v_{gs} = v_t$

- Subthreshold current has become a limiting factor in low voltage and low power chip design
  - Lower threshold voltage
  - Sensitive to temperature
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**Power and the circuit design styles**

- Circuit design styles
  - Nonclocked
    - Fully complementary logic, pass transistor, …
    - Slower, but consumes less power
  - Clocked
    - Domino, DCSL, …
    - Faster, but consumes more power

- Trade-off between performance and power
  - Faster logic consumes more power
Nonclocked - Fully complementary logic

- Aka. CMOS
- Active mode
  - Switching / short-circuit current
  - Glitches or spurious transitions due to different delays through different paths of the circuit
- Stand-by mode
  - Leakage current
  - High noise margin \(\Rightarrow\) can reduce the threshold voltage
  - Performance degrading factor
    - Large PMOS \(\Rightarrow\) Large input capacitance / weak output driving
Nonclocked - NMOS and pseudo-NMOS

- Aka. ratioed logic
- Pull-up resistance is higher than pull-down resistance
- Good for large fan-in gates
- Higher power dissipation than CMOS due to the static current

NMOS

Pseudo-NMOS
Nonclocked - DCVS

- Differential Cascade Voltage Switch
- A differential output signal is available
- Eliminates the static power in the ratioed logic
- \( f(\text{network 1}) = \sim f(\text{network 2}) \)
- Larger switched capacitance \( \Rightarrow \) higher switching power
  - Can be reduced by the sharing between two networks
Nonclocked - Pass transistor logic (PTL)

- AND: connected in series / OR: connected in parallel
- NMOS: good to transmit “0”, but not for “1”
- CPL: Complementary Pass-transistor Logic
  - Different input / output signals
  - Power-delay product is 10% better than CMOS

PTL: AND

CPL: NAND/AND

CPL: XOR/XNOR
**Clocked - Domino**

- Clock = 0: Output is precharged
- Clock = 1: Evaluated (conditionally discharged)
- Only implements non-inverting logic gates
- Good for large fan-in gates
- Clock switching $\rightarrow$ high power

Domino NAND
Clocked - DCVS

- Differential Current Switch Logic
- Clocked DCVS to reduce the internal node voltage swing
- T2, T3, T6, T7: Static latch
  - Sensing the difference of Q and Q'
- Clk = 0: Precharge Q and Q'
- Clk = 1: T9, T10, T11 switch on
  - T5, T6, T7, T8 are on
  - Q and Q' are discharging
  - Discharging rate given by NMOS tree
  - T5 or T8 is cut off and isolated from the tree
  - Low internal voltage swing / No static current
  - T5 / T8: increase output capacitance, but reduces effective internal capacitance
**Clocked - DCSL2**

- Output (Q, Q’)
  - precharged low unlike DCSL1 when CLK = 1
- NMOS tree is disconnected by T5 and T8
- Evaluation starts when CLK goes low
- Evaluation starts only after the outputs have crossed $V_{tn}$
Clocked - DCSL3

- Replace T9 and T10 in DCSL2 by T9
- T9 equalizes Q and Q’ when CLK goes high
- T5, T6, T7, and T8 are on
- Q and Q’ discharge to a voltage that is $V_{tn}$ or lower
Leakage conscious design - SATS

- SATS
  - Self-adjusting threshold voltage scheme
  - Measure the leakage of a representative MOS
  - If the measured value > the expected value
  - Decrease the back bias for NMOS, increase it for PMOS
    - $V_{th}$ will be increased
**Leakage concisous design - MTCMOS**

- Multithreshold CMOS
  - Uses both high- and low-threshold voltage MOSFETs
  - Active mode: SL is set to high / Sleep mode: SL is set to low
  - The “on” resistance of sleep transistors is small
  - Some designs only use either header or footer
  - Cell-based MTCMOS ➔ area penalty / easy to design
  - Block-based MTCMOS ➔ area efficiency / hard to design
Leakage conscious design - DTMOS

- Tie up the input to the back bias
- Control the depletion area
- See the DTMOS inverter
- **IN = 0**
  - NMOS turn off (normal $V_{th}$)
  - PMOS turn on (low $V_{th}$) by reduced depletion area
  - Low leakage to GND, while high speed switching
- **IN = 1**
  - NMOS turn on (low $V_{th}$) by reduced depletion area
  - PMOS turn off (high $V_{th}$)
  - Low leakage to VDD, while high speed switching
Special latches and flip-flops

- Most frequently used elements in digital VLSI
- Two energy dissipation components
  - Clock energy
  - Data energy
  - Clock change rate is much higher than data change rate
    - Focus on the clock to reduce the energy dissipation
- Attempotions
  - Reduce the gate capacitance connected to the clock
  - Reduce or increase # of trs to minimize the unnecessary internal node switching
Example of low power flip-flops

- A cascaded version of two single phase latches
  - Removes the internal phase splitting inverter

- Low power with static latch
  - Data is retained statically
Self-gating flip-flop

- Avoid clock switching when it is not necessary
  - Uses internally generated clock
  - Efficiency depends on the input data rate
Double edge flip-flop

- Uses both clock edges
  - Can reduce the clock speed by half
  - Small area overhead

(a) Single edge triggered flip-flop.

(b) Double edge triggered flip-flop.
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**Sizing - Inverter chain (I)**

- The simplest sizing problem
- Find an optimal length from delay and power perspective

**Assumption**
- Fixed P/N size ratio for all inverters \(\Rightarrow\) Same rise/fall time
- Fixed stage ratio \(\Rightarrow\) \(K\)

**Simple analysis:** \(\frac{C_i}{C_{i-1}} = K \Rightarrow \frac{C_N}{C_0} = K^N\)
- \(N = \ln\left(\frac{C_N}{C_0}\right) / \ln K\)
Sizing - Inverter chain (II)

- Delay
  - \( D = NKd = \ln(C_N/C_0) \times (K / \ln K) \times d \)
  - \( d \): intrinsic delay of the inverter under a single load
  - \( D \) is minimized when \( K = e \)

- Power
  - \( P_i = KP_{i-1} \)
  - \( P = IV \)
  - \( V \): unchanged
  - \( I = C(dv/dt) \)

\[
P = \sum_{i=0}^{N-1} P_i = \sum_{i=0}^{N-1} K_i P_0 = \frac{K^N - 1}{K - 1} P_0
\]

\[
P_0 = C_1 V^2 f + \pi S_0 f = Kf(C_0 V^2 + \frac{\tau}{K} S_0)
\]

\[
P_0 \propto K, K_n = C_N / C_0
\]

\[
P \propto \frac{K}{K - 1}
\]
Sizing - Inverter chain (III)

- Power/Delay vs. K

- Delay is minimized when K = e
- Power is approaching to 1 as K increases
  - Higher K means a shorter chain ➔ Less switching capacitance
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Circuit-level power analysis

- SPICE is the de facto power analysis tool
  - Simulation Program with IC Emphasis
  - A lot of SPICE related literatures and simulators
    - HSPICE, PSPICE, …
  - The reference for the higher abstraction levels
  - Accurate, but slow

- Recently, faster analysis tools were introduced
  - E.g. PowerMill, Spectre, …
  - Still accuracy is inferior to SPICE
**SPICE basics**

- Solving a large matrix of nodal current using Krichoff’s Current Law (KCL)
- Primitive elements
  - Registers, capacitors, inductors, current sources, voltage sources
- More complex elements
  - Such as diodes and transistors
  - Constructed from the primitive elements
- Analysis modes
  - DC analysis
  - Transient analysis
SPI CE power analysis

- Can estimate all types of power
  - Dynamic / Static / Leakage
- Not feasible for the entire chip due to the computation complexity
  - Can be used as a characterization tool for higher abstraction level analysis
- Can consider process and other parameter’s variation
  - BEST / TYPICAL / WORST
Discrete transistor modeling / analysis

- To speed up the analysis
  - Lose accuracy

- Typical methods
  - Circuit model
    - Approximate the complex equations into a linear equation
  - Tabular transistor model
    - Express the transistor models in tabular forms
  - Switch model
    - Consider a transistors as a two-state switch (on / off)
Circuit model

\[ I_{ds} = f(V_{gs}, V_{ds}) \]

\[ \approx f(V_{gso}, V_{dso}) + \frac{\partial}{\partial V_{gs}} f(V_{gso}, V_{dso})(V_{gs} - V_{gso}) + \frac{\partial}{\partial V_{ds}} f(V_{gso}, V_{dso})(V_{ds} - V_{dso}) \]

\[ i_{ds} \approx i_0 + g_m v_{gs} + r_{ds} \]

- The linear equation should be numerically evaluated whenever the operating points change.
Tabular transistor model

- Pre-compute a current table
- Look up the table instead of solving an equation
- Table format

<table>
<thead>
<tr>
<th>$V_{ges}$</th>
<th>$V_{dso}$</th>
<th>$i_{ds}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>10</td>
</tr>
</tbody>
</table>

- One-time characterization effort for each MOS
- Event-driven appraoch can be used for speed-up
- Nearly two orders of magnitude improvement (speed, size)
Switch model

\[ I_{ds} = f(V_{gs}, V_{ds}) \]

\[ \approx f(V_{gso}, V_{dso}) + \frac{\partial}{\partial V_{gs}} f(V_{gso}, V_{dso})(V_{gs} - V_{gso}) + \frac{\partial}{\partial V_{ds}} f(V_{gso}, V_{dso})(V_{ds} - V_{dso}) \]

- RC calculation for timing
- Power is estimated from the switching frequency and capacitance
- Further speed-up, but less accuracy
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Power characterization for cell library

- Circuit-level power analysis is time consuming
- Need to speed up with reasonable accuracy loss
- Levels beyond gate level will be discussed later
- Partially similar to delay characterization
- Dynamic power
  - Capacitive power dissipation
  - Internal switching power dissipation
- Leakage power
  - Accuracy depends on the model of circuit simulation
  - Iterative analytic estimation
  - Simulation based approach
**Power characterization flow**

- Accuracy vs. speed
  - Too many input patterns → Too many simulation runs
  - Too many input patterns → probabilistic analysis

```
010110
110111
000100
........
```

- Circuit Simulator → A large # of current waveforms → Average → Power
- Average → Probability Values → Analysis tools → Power
Simulation-based cell characterization

- Parameters
  - Input pattern (logical value)
  - Input slope
  - Output loading capacitance
  - Process condition
- Total # of runs of simulation is the multiplication of the possible number of values of each parameter
  - Some parameters are continuous
    - Input slope, output loading capacitance
    - Piece-wise linear approximation is widely used
  - Process / operation condition: BEST / TYPICAL / WORST
Example: 2-input NAND (1)

- Possible input patterns
  - Dynamic power
    - A | B | C | Power
      - 1 | r | f | ?
      - 1 | f | r | ?
      - r | 1 | f | ?
      - f | 1 | r | ?

- Static power
    - A | B | C | Power
      - 0 | 0 | 1 | ?
      - 0 | 1 | 1 | ?
      - 1 | 0 | 1 | ?
      - 1 | 1 | 0 | ?

8 simulation runs!
Example: 2-input NAND (II)

- Input slope
  - Depending on the predecessor

- Capacitance
  - Depending on the successor
  - Proportional to the # of fan-outs
  - If we consider four points for capacitance

- Total # of simulation runs for a single input
  - \(2 \text{ (rise / fall)} \times 4 \text{ (# of input slopes)} \times 4 \text{ (# of capacitance points)} = 32 \text{ points}\)
Example: 2-input NAND (III)

- Process / operation condition
  - Temperature
  - Process variations such as doping density
  - Typically use 3 conditions are widely used

- Total # of simulations
  - For dynamic power
    - \((2 \times 2) \times S \times C \times P\)
  - For static power
    - \(2^2 \times P\)
Additional factors to be characterized

- Output slope
  - Used as an input slope of the successor
  - Need to know for each simulation point

- Input capacitance
  - Used for computing the total output capacitance of the predecessor
  - Can be estimated by the area of gate (W/L) and $t_{ox}$
  - Parasitics: $C_{gs} / C_{gd}$

- All the information should be included in the library
Tool flow

- Library information
- Circuit netlist
- Slope/Cap information

input pattern generator

Circuit simulator

Simulation Analyzer

- Synthesis library
- Library generator
- Simulation library
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Probability-based power estimation

- Pre-requisite to move to module 8
- If we ignore internal capacitance of a logic gate
  \[ P_{\text{avg}} = \frac{1}{2} V_{\text{dd}}^2 C f \]
- Parameters
  - C: switched capacitance
  - f : the frequency of operation
    - For aperiodic signals: the average # of signal transitions per unit time
    - Called signal activity
- Our concern
  - How to estimate f in a probabilistic manner
Modeling of signals

- To model the digital signals, need to know
  - Signal probability
  - Signal activity
- $g(t)$, $t \in (-\infty, \infty)$
  - A stochastic process that takes the values of logical 0 or 1
  - Transitioning from one to the other at random times
  - SSS: Strict-Sense Stationary
  - Mean ergodic
    - Constant mean with a finite variance
    - $g(t)$ and $g(t+\tau)$ become uncorrelated as $\tau \to \infty$
Signal probability and activity

- Signal probability

\[ P(g) = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{+T} g(t) dt \]

- P(g=1) : signal probability

- Signal activity

\[ A(g) = \lim_{T \to \infty} \frac{n_g(T)}{T} \]

- \( n_g(t) \): # of transitions of \( g(t) \) in the time interval between \(-T/2\) and \(+T/2\)
Signal probabilities of simple gates

- Assumption
  - $g_1, g_2, \ldots, g_n$ are independent
- Output signal probability
  - Determined by the given boolean function
  - NOT: $1 - P$
  - AND: multiply
  - OR $\rightarrow$ NOT (NOT (OR))

- Inverter
- AND gate
- OR gate
**Signal probability calculation (I)**

- By Parker and McClusky
- Algorithm: Compute signal probabilities
  - **Input**: Signal probabilities of all the inputs to the circuit
  - **Output**: Signal probabilities of all nodes of the circuit
  - **Step 1**: For each input signal and gate output in the circuit, assign a unique variable
  - **Step 2**: Starting at the inputs and proceeding to the outputs, write the expression for the output of each gate as a function (using standard expressions for each gate type for probability of its output signal in terms of its mutually independent primary input signals)
  - **Step 3**: Suppress all exponents in a given expression to obtain the correct probability for that signal
Signal probability calculation (II)

- Step 3 for protecting recovergent fanout
  - *W/o* step 3, the reconvergent fanout node may have a signal probability higher than 1

- A boolean function $f$
  - $P(f) = \sum_{i=1}^{p} \alpha_i (\prod_{k=1}^{n} P^{m,k} (x_k))$
  - $n$: # of independent inputs
  - $p$: # of products
  - $\alpha_i$: some integer
  - Called as the sum of probability products of $f$
Signal probability calculation (III)

- \( P(f) = \sum_{i=1}^{p} \alpha_i \left( \prod_{k=1}^{n} P^{m_{i,k}}(x_k) \overline{P^{l_{i,k}}}(x_k) \right) \)

- \( \overline{P(x_i)} = P(\overline{x_i}) = 1 - P(x_i) \)
- \( m_{i,k} \) and \( l_{i,k} \) are either 0 or 1, cannot be 1 simultaneously

- Canonical sum of probability product of \( f \)
  - \( P(f) = \sum_{i=1}^{p} \left( \prod_{k=1}^{n} P^{m_{i,k}}(s_k) \right) \)
  - \( s_k = x_k \) or \( x'_k \)
Signal probability calculation: Example

- \( y = x_1x_2 + x_1x_3, \) \( x_i, \) \( i = 1, 2, 3 \) are mutually independent
- \( z = x_1x_2' + y \)
- \( P(y) = P(x_1x_2) + P(x_1x_3) - P(x_1x_2)P(x_1x_3) \)
  \( = P(x_1)P(x_2) + P(x_1)P(x_3) - P(x_1)P(x_2)P(x_3) \)
- \( P(z) = P(x_1x_2') + P(y) - P(x_1x_2')P(y) \)
  \( = P(x_1)P'(x_2) + P(x_1)P(x_2) + P(x_1)P(x_3) - P(x_1)P(x_2)p(x_3) - \)
  \( P(x_1)P'(x_2)(P(x_1)P(x_2) + P(x_1)P(x_3) - P(x_1)P(x_2)P(x_3)) \)
- \( P(x_2)P'(x_2) = P(x_2) (1 - P(x_2)) = 0 \)
- \( P(z) = P(x_1)P'(x_2) + P(x_1)P(x_2) + P(x_1)P(x_3) - P(x_1)P(x_2)p(x_3) - \)
  \( P(x_1)P'(x_2)P(x_3) \)
Signal probability using BDD (1)

- BDD: Binary Decision Diagram
- Shannon’s expansion
  \[ f = x_i \cdot f(x_1, \ldots, 1, x_{i+1}, \ldots, x_n) + \overline{x_i} f(x_1, \ldots, 0, x_{i+1}, \ldots, x_n) \]
- Cofactors w.r.t. \( x_i \) and \( x'_i \)
  \[ f_{x_i} = f(x_1, \ldots, 1, x_{i+1}, \ldots, x_n) \]
  \[ f_{x'_i} = f(x_1, \ldots, 0, x_{i+1}, \ldots, x_n) \]
- Example
  \[ f = ab + c \]
Signal probability using BDD (II)

- \( P(f) \)
  - \( P(x_1 \cdot f_{x_1} + x_1 \cdot f_{\overline{x_1}}) \)
  - \( P(x_1 \cdot f_{x_1}) + P(x_1 \cdot f_{\overline{x_1}}) \)
  - \( P(x_1) \cdot P(f_{x_1}) + P(x_1) \cdot P(f_{\overline{x_1}}) \)

- A depth first traversal of BDD, with a post order evaluation of \( P(.) \) at every node is required for evaluation of \( P(f) \)
Summary

- Low power is a must
  - Battery lifetime / Thermal problems
- Leakage power is getting dominant
  - Design style also follows the trend
- Solution for delay may not work for power
  - Sizing problem of inverter chain
- Power characterization for higher level power analysis
  - Similar to delay characterization, but different
- Probability-based power estimation is often required
  - Accuracy / speed trade-off
References

- http://public.itrs.net
Assignment

- Study other circuit design styles for low power design
- What are the differences between delay characterization and power characterization?