Low-Power Equalizer VLSI Implementation for xDSL

Jun-Dong Cho and Jin-Woo Kim

Dept. of ECE, Sungkyunkwan University jdcho@skku.ac.kr

1 Introduction

Today's environment is ripe for emergency of Digital Subscriber Line (DSL) technologies [1]. xDSL service promises to dramatically increase the speed of copper wire-based transmission systems without requiring expensive upgrades to the local loop infrastructure. In xDSL technology, however, tremendous channel equalization is needed for broadband transmission rates. Channel equalization requires processing power so high that power consumption and clock speed become major design challenges [2].

This paper describes techniques to implement low-power adaptive equalizers for ASIC implementation of xDSL. Section 2 addresses the conventional FEQ without considering low-power design. In Section 3, our low-power techniques are described. In Section 4, we compare the performance and power consumption between conventional equalizer and our low-power one. Section 5 draws a conclusion.

2 Conventional FEQ without Targeting Low-Power Design

Block diagram of general 1-tap FIR (Finite Impulse Response) filter that is the main component of FEQ, is shown in Fig-1.

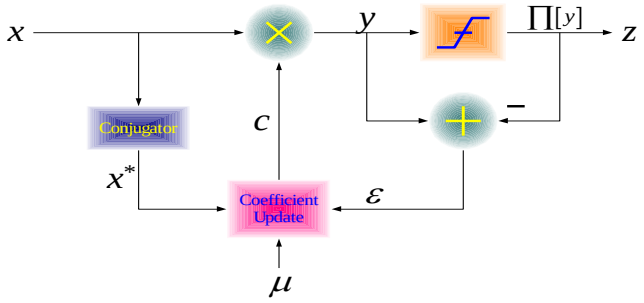

Fig-1 1-tap LMS FIR Filter

In Fig-1, input Sequence x is output of FFT's one tap. Important internal sequences are ε (error sequence) and c (coefficient sequence). Finally, y (output sequence) is multiplied by c. LMS adaptive algorithm is formulated as follows.

$$c(j+1,k) = c(j,k) - \mu\varepsilon(j,k)x^*(j,k) \qquad (1)$$

3 Our new Low-Power Algorithm to Equalizer FEQ

Our run-time power reduction technique is composed of three categories. The proposed entire architecture is illustrated in Fig-2, where some blocks are inserted and modified in concern of low power.

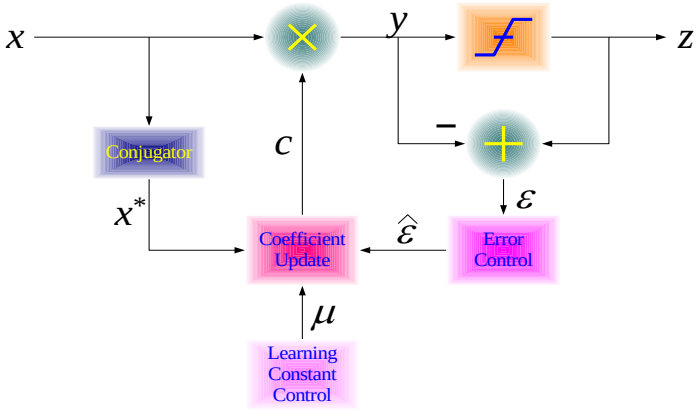

Fig-2 Low-Power FIR Filter Architecture

1) Error Control Block : This block uses two modes of update-operation for low power. The first is called the 'Burst-Mode Update', which is an error update when a certain threshold value is exceeded. Next one is called the 'Step-Mode Update' in which power-of-2 value of $\hat{\varepsilon}$ can be multiplied in 'Coefficient Update' block with only an addition.

2) Learning Constant Control Block : The learning constant control block varies μ (learning constant). Then power reduction is attained because switching activity (frequency) during multiplication is reduced. A new method of varying μ is as in (2). This enables to make μ into power-of-2 number system. Thus, division is substituted by exponent subtraction.

$$\mu(k) = \mu(k-1)/2, \quad \text{if symbol\_time \% 128} = 0 \qquad (2)$$

3) The Coefficient Update Block : The Coefficient Update block requires two multipliers and an adder. However, this block calculates coefficients with only 3 additions instead of 2 multiplications and 1

addition, because all number system is changed into power-of-2 number system as described before. The two series of additions can be replaced by a CSA (Carry Save Adder) that enables more power reduction. As a consequence, 2 multipliers are replaces by 2 adders or 1 CSA.

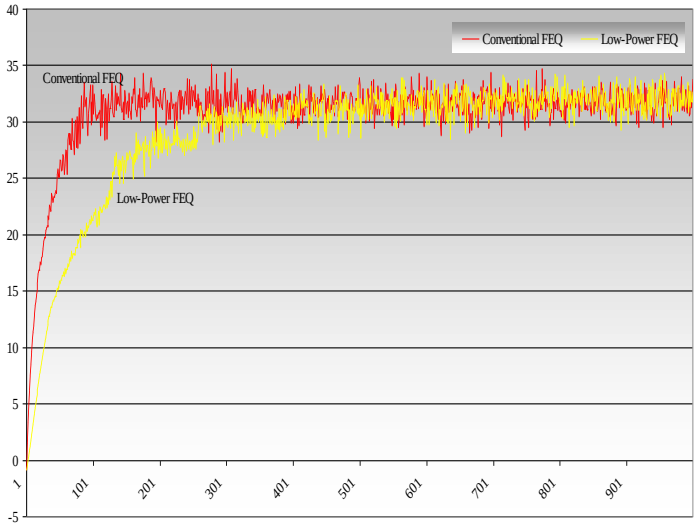

Fig-3 Comparison between Conventional FEQ and Low Power FEQ

4 Simulation of Low-Power Equalizer and Comparison

ADSL system is simulated 1000-symbol time with channel SNR (Signal to Noise Ratio) 40dB. Tested channel is CSA-6. The performance in equalizers is measured by both output SNR and convergence time. An illustration of comparison between conventional FEQ and low-power FEQ is shown in Fig-3. Fig-3 shows that low-power FEQ is similar to conventional one in terms of performance. The output SNR of low-power FEQ is close to or higher than the SNR of conventional one, even though the convergence time of low-power FEQ is slower than the time of conventional one. This performance is tolerable in ADSL FEQ training specification. The power consumption of each component is provided by [5].

Table-1 Power consumption Comparison

Component	**Power Consumption (Normalized to FEQ)**
Conventional FEQ	1
Low-Power FEQ	**0.806**

From Table-1 and Fig-4, power reduction attained by replacing multipliers by adders, is obtained by 22% and other hardware component overhead increases power consumption by 2.6%. Therefore, the power reduction of low-power FEQ is about 19.4%. Because this result does not include run-time power reduction, the entire power consumption of low-power FEQ will be less than be the result here.

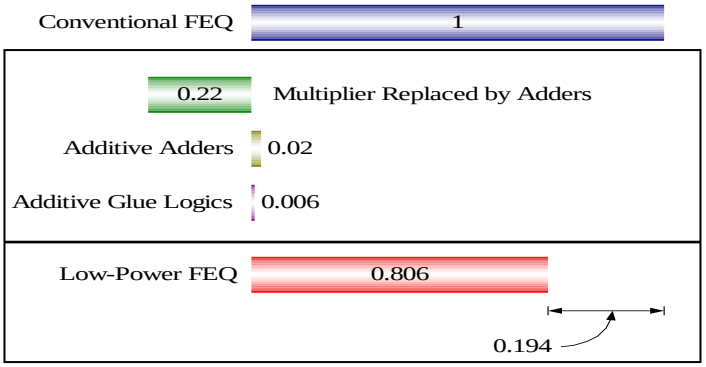

Fig-4 Power Reduction from Conventional FEQ to Low-Power FEQ

5 Conclusion

In this paper, a novel low-power equalizer is implemented and simulated. At a slight degradation in performance in terms of SNR and convergence time, power consumption is reduced and the faster equalizer is realized with replacing high-strength multiplier by low-strength adder along with approximation method. The slight performance degradation is not critical. Moreover, varying μ value method forces to improve the SNR and shortens the convergence time without using many hardware component overheads.

References

[1] *xDSL Local Loop Access Technology*, 3Com Technical Paper 500624-002, June, 1998

[2] Kamran Azadet et Al, "Low-Power Equalizer Architectures for High-Speed Modems," *IEEE Communication Magazine*, pp. 118-126, Oct, 1998

[3] Abdellatif Bellaouar, Mohamed I. Elmasry, *Low-Power Digital VLSI Design*, Kluwer Academic Publishers, 1996

[4] Walter Y. Chen, *DSL : Simulation Techniques and Standards Development for Digital Subscriber Line System*, Macmillan Technical publishing, 1998

[5] Anantha P. Chandrakasan, Robert W. Broderson, *Low Power Digital CMOS Design*, Kluwer Academic Publishers, 1995